PROTOTYPE OF WATER DAM SYSTEM BY USING FPGA PLATFORM

Choong Yi Ming, Ahmad Mu'az Mohaspa and Wan Rahiman[1]

School of Electrical and Electronic Engineering
Universiti Sains Malaysia, Engineering Campus
Pulau Pinang, Malaysia.

Corresponding Author's Email: [1]wanrahiman@usm.my

ABSTRACT: A water dam system is a promising system which uses the aid of sensor to detect the real time depth of stream by measuring the height of the buoyant floating on the water. The goal of this project is to design a robotic water dam system which can raise its floodgate or gate after receiving the commands from user. It is designed to detect the water level and notify the user immediately with the aid of notification system hence user could command to raise or close the floodgate. The research paper demonstrates a prototype of a working and operational water dam system.

KEYWORDS: *FPGA, Water dam system, Frequency divider*

1.0 INTRODUCTION

This document contains the guidelines extended abstract preparation. Dam or water dam is a huge structure which can be found across a river to store water. Tosun H. (2019) described dam has several crucial functions as it provides water for human consumption and also industrial processes. Also, dam can act as generator to generate hydroelectric power. Besides, it can function as floodgate to reduce peak discharge of floodwater due to thunder storm or heavy snow and increase the depth of river water to allow navigation of ships and cruises as was mentioned by Tortorelli R. L. (1985).

Nahi M. K. (2018) explains some features that aid in the function of dam include movable gates and valves which function to control the release of surplus water downstream. In Brown at al. (2009) and Burke at al. (2009), dam is sometime known as central structure in a multipurpose scheme designed to conserve water.

The field-programmable gate array (FPGA) is a semiconductor device that can be programmed after manufacturing. The procedure had been explained in Buldu A. (2016), it is also known as an integrated circuit which can be designed by user after manufacturing hence it is programmable. Combinational functions or simple logic gates could be configured to perform in FPGA with the comprehensive explanation in Altera (2013). Most of the FPGA could be reprogrammed to run varied logic functions with the aid of memory elements such as simple flip-flops, also it allows flexible reconfigurable computing as performed in computer software. Grout I. (2008) explains sequential logic circuit based on combination logic elements (latches and flip-flops that will be grouped together to form register).

2.0 PROJECT DESCRIPTION

The task given for this project is to design a system which comprise of digital circuit combining analogue circuit with theme given 'Robotic'. The control signals to movement of motors should be provided by a FPGA board. The purpose of this project is to design a digital circuit with the aid of Altera Quartus II 13.0 Web Edition combining analogue circuit to function a system designed with theme 'Robotic'. Altera Quartus II 13.0 Web Edition is a programmable logic device design software developed by Intel where it can aid in designing circuits. Besides, an Altera DE2-115

Development and Education Board, a type of field programmable gate array (FPGA) is used to fulfil our requirements in the project.

In this project, we decided to use two stepper motor to produce preferred outputs. Also, we will use FPGA board to produce outputs for IC ULN2003 which function as motor driver for 35BY48L-97 stepper motor. Diagram below illustrate the effect of sequence on rotational motion of the stepper motor applied in this project which known as full step (low torque) with one phase HIGH.

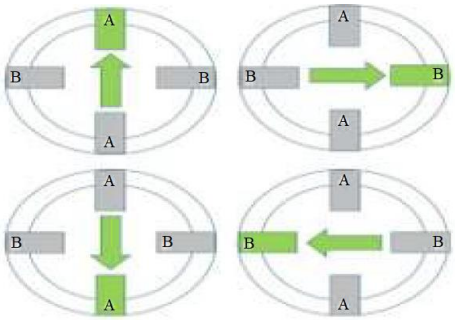

Figure 1: Full Step (Low Torque) with one phase HIGH.

We have decided to design the stepper motor rotate in full step (low torque) with one phase HIGH motion. The step angle of the stepper motor used is 7.5 degree per step, hence we decided to make it move 6 steps per click so that it could rotate 45 degree per click and raise the gate 25% from its max opening of the gate. The reason to do so is to have a better control of the output of stepper motor. Assuming that the input pins controlling the 4 phases of stepper motor be A, B, C and D. The input for each phases is shown in Table 1 to ensure the motors move as preference

Table 1: Stepper Motor Steps and Inputs for 45 Degree Rotation

STEP	**INPUT**			
	A	B	C	D
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1
5	1	0	0	0
6	0	1	0	0

Besides, we also design a clock pulses generator which function to produce 6 clock pulses by pressing input key once. The output of the clock pulses generator will be connected to the clock of the modified bidirectional ring counter and shift register which function to provide outputs for IC ULN2003 motor driver so that it could change its state for 6 times. Furthermore, we also designed a frequency divider which function to reduce the high built in 50MHz frequency of the FPGA board to preferred range which is 3Hz to 6Hz.

3.0 METHODOLOGY

A. Digital Schematic Circuit

The digital schematic circuit of the Water Dam System is designed through combination of several systems. The systems include Display System, Notification System, Security Lock System, Frequency Divider, Clock Pulses Generator and Modified Bidirectional Shift Register and Ring Counter.

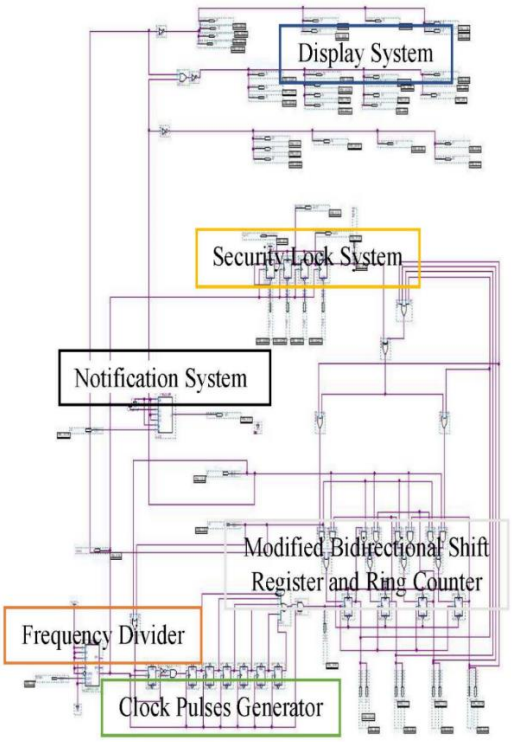

Figure 2: Digital Schematic Circuit of the Water Dam System.

B. Security Lock System

The output will only be HIGH when the user has entered the correct password and the water dam system could only function when the output from the security lock system is HIGH else the dam won't be able to function. When all of the CLEARs are activated indicating that the passwords entered are incorrect and the system will stop functioning.

Inversely, when the passwords entered are correct the CLEARs will be deactivated and the output will become HIGH. The LEDs from each D flip-flop will become HIGH and light up when the password entered is correct. However, after the correct passwords are entered the user is not allowed to change the pin of the passwords.

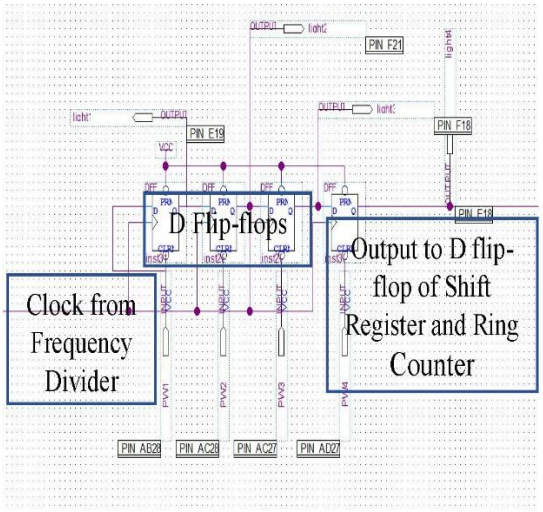

Figure 3: Digital schematic diagram for Security Lock System.

C. Frequency Divider

The default frequency from the FPGA board used in the system is 50MHz which is significantly high for stepper motors used in the system. So, an IC 74292 is used to reduce the frequency so that the stepper motor could work. Table 3 shows the function table for IC 74292.

Table 3: Function Table of IC 74292.

H	L	H	H	L	2^{22}	4194304
H	L	H	H	H	2^{23}	8388608
H	H	L	L	L	2^{24}	16777216

The connection of IC 74292 in Table 3 is 'HLHHH'. Hence, according to this table above we can conclude that the frequency is divided by 2^23 and the output of the frequency after going through IC 74292 is :

$$Clock\ frequency = \frac{50M}{2^{23}} Hz \approx 5.96Hz$$

As a result, the final clock frequency is reduced to approximately 5.96Hz which is suitable for the operation of stepper motor.

4.0 RESULTS AND SIMULATIONS

A. Clock Pulses Generator

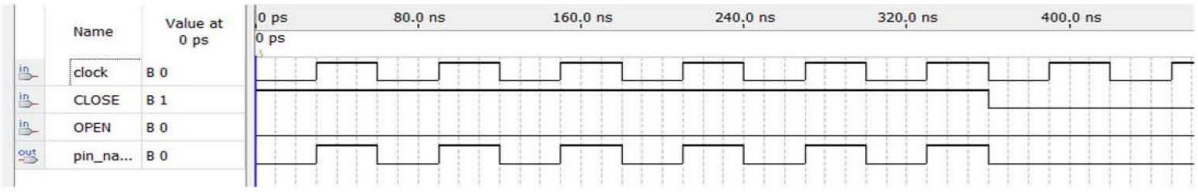

Figure 4: Simulation waveform of clock pulses generator when 'CLOSE' is triggered.

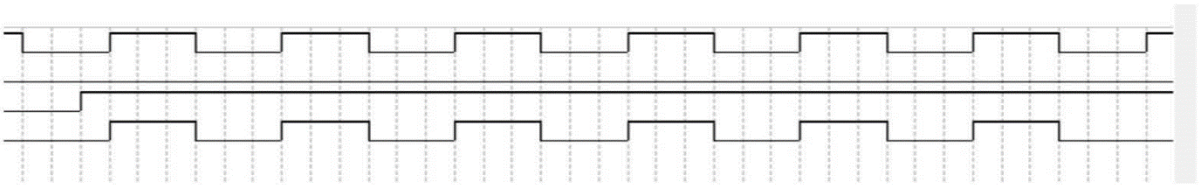

Figure 5: Simulation waveform of clock pulses generator when 'OPEN' is triggered.

The simulation showed that the clock pulses generator only produces six pulses or clocks for the Modified Bidirectional Shift Register and Ring Counter so that the stepper motors could rotate 45 degree which is equivalent to 25% of the max opening of the gate.

B. Security Lock System

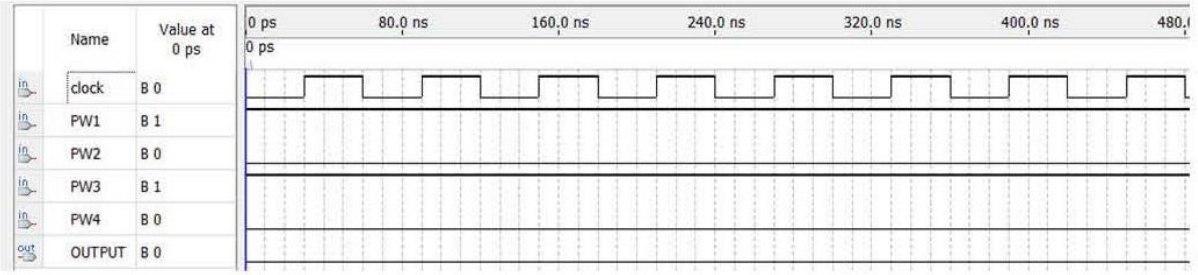

Figure 6: Simulation waveform of Security Lock System when passwrords entered are incorrect.

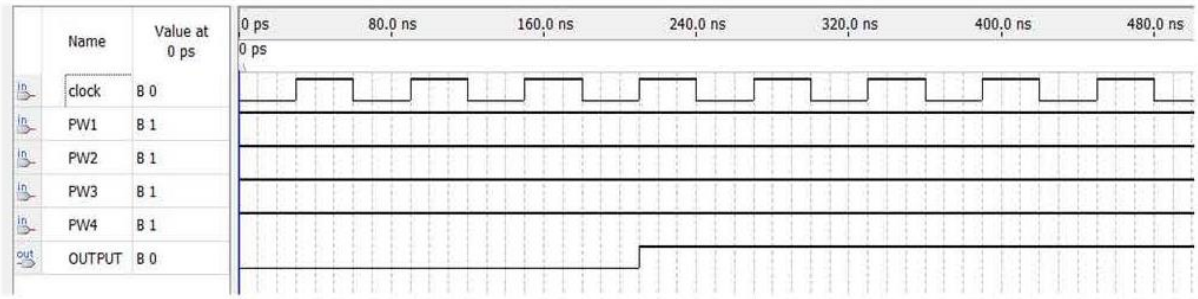

Figure 7: Simulation waveform of Security Lock System when passwords entered are correct.

From the Figure 6 and 7, we could see that when the passwords entered are incorrect the final output will be LOW ; inversely when the correct passwords are entered the final output will be HIGH and the water dam will start to function.

5.0 DISCUSSIONS

In this project, we need to build the digital circuit by using the Altera Quartus II 13.0 Web Edition software. We learnt how to use the software so that we can build the digital circuit that we want, do simulation for the digital circuit drawn and assign input and output pin on the FPGA Board. Next, we also learnt that the stepper motor has a few steps for it to work depending on the how many phases that being magnetized. Furthermore, we realised that the IC ULN2003 will amplify the current from its input to the output connected to stepper motor. Hence, the current coming from the GPIO pins is amplified to drive the stepper motor. Last but not least, learnt how to build a mechanical part of our by referring the system that we just learnt that is the two axes gimbal system.

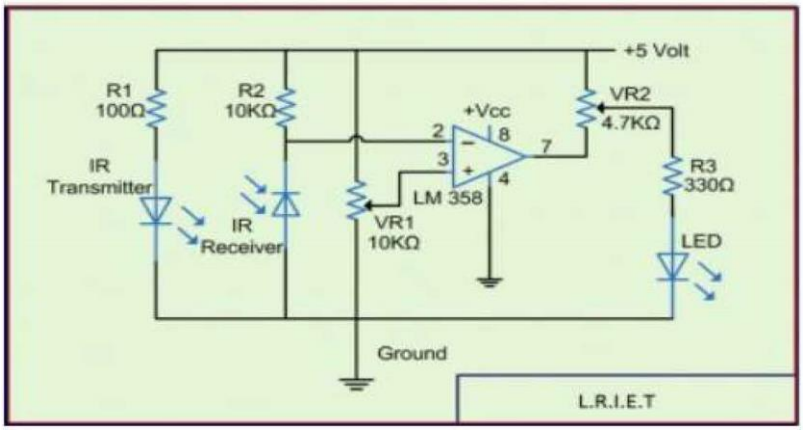

Figure 23: IR Sensor circuit.

When the IR receiver does not receive a signal, the potential at the inverting input goes higher than that non-inverting input of the comparator IC (LM339). Thus the output of the comparator goes low, but the LED does not glow. When the IR receiver module receives signal to the potential at the inverting input goes low. Thus the output of the comparator (LM 339) goes high and the LED starts glowing. Resistor R1 (100), R2 (10k) and R3 (330) are used to ensure that minimum 10 mA current passes through the IR LED Devices like Photodiode and normal LEDs respectively. Resistor VR2 (preset=5k) is used to adjust the output terminals. Resistor VR1 (preset=10k) is used to set the sensitivity of the circuit Diagram.

6.0 CONCLUSIONS

In conclusion, the tasks given and the objectives of the project were achieved. We implemented a variety of systems in order to complete the project. The systems included are Display System , Notification System, Security Lock System, Frequency Divider, Clock Pulses Generator and Modified Bidirectional Shift Register and Ring Counter. Each system and features has specific function which makes the Water Dam System complete. Also, we added mechanical part which is the application of the project, Water Dam System. We designed the prototype through the idea of pulley system where there are strings attach to the stepper motors and the floodgate. This enable user to raise or close the gate as user preference. The floodgate will raise or close up to 25% of its max opening once a "CLOSE' or 'OPEN' is triggered. The Notification System will also notify the user once the water level is high or low so that user could decide whether to raise or close the floodgate. Besides, for security purpose, a Security Lock System is included to ensure the Water Dam is in safe hand. However there are some improvement could be made as we could use more components such as buzzer to strengthen the Notification System.

7.0 ACKNOWLEDGEMENT

This project was supported by the Universiti Sains Malaysia under the Bridging Grant 304.PELECT.6316121. We would like to thanks the university for allowing us to use the FPGA Laboratory at the School of Electrical and Electronic Engineering, Universiti Sains Malaysia to complete the project.

8.0 REFERENCES

Tosun H. (2019). *Dam Engineering*, IntechOpen

Tortorelli R. L. & Bergman D. L. (1985). Techniques for estimating flood peak discharges for unregulated streams and streams regulated by small floodwater retarding structures in Oklahoma. *U.S. GEOLOGICAL SURVEY Water-Resources Investigations Report 84-4358.* Oklahoma Department of Transportation

Nahi M. K. (2018). Design and Analysis of Lifting Mechanism in Water Dams Using Composite Materials. *International Journal of Applied Engineering Research, 13(13), 11045-11053*

Brown P. H., Tullos D., Tilt B., Magee D. & Wolf A. T. (2009). Modeling the costs and benefits of dam construction from a multidisciplinary perspective. *Journal of Environmental Management, 90(3), S303-S311*

Burkea M., Jorde K. & Buffington J. M. (2009). Application of a hierarchical framework for assessing environmental impacts of dam operation: Changes in streamflow, bed mobility and recruitment of riparian trees in a western North American river. *Journal of Environmental Management, 90(3), S224-S236*

Buldu A. & Yildiz K. (2016, July). A Circuit Design by Using an Infrared Sensor Transmitter and Pic16f628 to Measure the Pulse Rate of the Driver. *Measurement and Control, 49(6), 191-196*

Altera (2013). DE2-115. *User Manual. World Leading FPGA Based Product and Design Services.* Terasic Technologies Inc.

Grout I. (2008). Introduction to Digital Logic Design with VHDL. In *Digital Systems Design with FPGAs and CPLDs, pages 333-474*