ELECTRONIC MAILBOX DESIGNED WITH FPGA PLATFORM

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ABSTRACT: An electronic mailbox is a device proposed to detect letter delivered by postman when the mailbox is opened or closed to notify the user for their new mail. The goal of this project is to make a mailbox model that can calculate the amount of mailbox opened by postman and lights up the yellow or red LED and buzz the buzzer to indicate an existing mail inside the mailbox. It is design to demonstrate the feasibility of using a Field Programmable Gate Array (FPGA) to implement custom hardware functionality. The present hardware consists of an infrared sensor (IR), a buzzer, seven segment display, FPGA and pushbuttons. This research paper demonstrates our proposed ideas, describes the design of a smart mailbox, the prototype, and the current results of work.

KEYWORDS: *FPGA, Mailbox, Infrared (IR) sensor*

1.0 INTRODUCTION

Nowadays, the world is full of science and technology, they replace traditional items in many ways and fields. One of the most significant change is the propose of Electronic Mail (e-mail). Nightingale et al. (2008) discussed two types of communication within companies by means of classical communication and modern communication. Email has become an indispensable part of daily business activities in nearly all aspects of commerce. Therefore, a mailbox that can notify the user for their new mail is solutions are being worked out. Suhaimi M. S. (2012) has developed mailbox integrated with GSM to notify the receipts on the incoming mail. This smart mailbox is a way to help notify the user to collect their mail on time to avoid them forgot to collect it especially when important letter was delivered as it will outcome a problem to them. FPGA based system is chosen to programme this project as it is very flexible, reusable, and quicker to acquire. The book by Ndjountche T. (2016) explains that the logic blocks can be configured to perform complex combinational functions, or merely simple logic gates like AND and XOR. In this Project, the FPGA board used is Altera DE2-115.

2.0 PROJECT DESCRIPTION

The overall concept of this project is the mailbox will display the number of mailbox opened by postman, so the user knows how many time the postman have come to deliver their mail and collect it before the number will keep increasing. The IR sensor detect the letter inside the mailbox and it will output a signal to yellow LED. The yellow LED lights up and the buzzer in the user house buzzes to notify them to collect their mail immediately. If they still not collect their mail until the number display show seven due to the fact that the system is designed using 3-bit up-counter that counting from one to seven, the yellow and red LED will light up to give a warning to users for their uncollected mail.

A. Body Specification

The mailbox's body designed is a cuboid equipped with two doors which located at the both front and back of the body. Both doors with the hinge at the bottom which makes the door can be opened vertically downward and be closed vertically upward.

Two pushbuttons are attached to the upper part of the inner wall of mailbox's body with the pressable part facing out and the bottom part of the pressable part parallel with the outer vertical wall. This arrangement enable the pushbutton to be pressed when the door closed and depressed when the door opened. The pushbutton attached to the front door is called by front pushbutton and the one attached to the back door is called by back pushbutton.

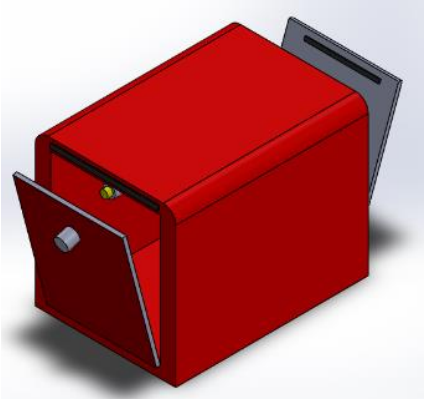

Figure 1. Idea of Mailbox Body

3.0 PROGRAMMING OF FPGA BOARD

We are taking instructions and advise given in Cofer R. C. (2005) in order to develop the prototype by using FPGA platform. Through the procedure mentioned, the steps and stages of the process are as:

A. Detection of Mails by IR Sensor

An infrared sensor is an electronic device that emits in order to sense some aspects of the surroundings. An IR sensor will be attached at the bottom of the mailbox at the pre-cut hole. The distance of detection is adjusted to just 3cm in order to suit the application. When there is mail, despite the number, inside the mailbox, it block the infrared wave that emitted by the IR sensor and reflect it back to the receiver. This outputs a "HIGH" to the Yellow LED.

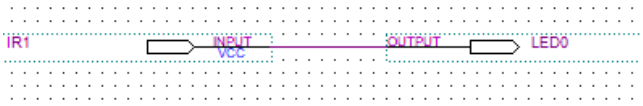

Figure 2. Block Diagram of circuit involving IR Sensor

B. Stop the counter at $(111)_2$

The Red LED lights up when the counter reaches $(111)_2$ which is 7 in decimal indicates MAXIMUM. Therefore, even if the postman continues open the mailbox and inserts the mails, the Red LED has to be lighted up until the host opens the back door to collect all the mails.

In order to achieve that, the counter have to be stopped when it reached $(111)_2$. Some additional gates contribute to this application. The output $(111)_2$ is connected to a NOT gate then to a 2 inputs AND gate with another input from the front pushbutton which acts as the clock for the 3-bits up counter. Through this way, when output $(111)_2$ reached, the "HIGH" output will be transformed to "LOW" after passing through the NOT gate. Then the AND gate will not allow any signal to pass through even when the clock(front pushbutton) still activated. This condition will continues until the back pushbutton is unpressed and activate the CLEAR pin.

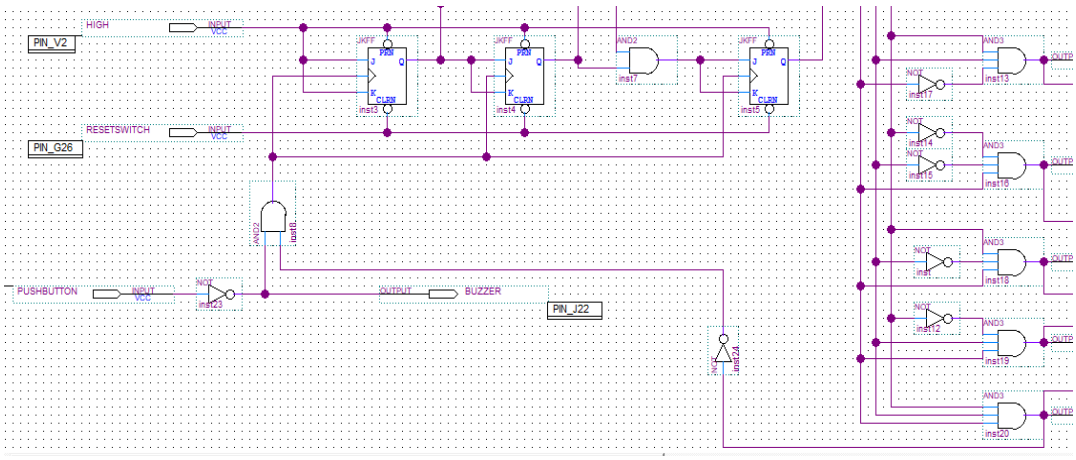

Figure 3. Block Diagram showing the additional gates

C. Application of Buzzer

A 12V DC buzzer is connected to the front pushbutton and located inside the house. It acts as the output of the input signal from front pushbutton. When the front pushbutton is unpressed, which is when the postman opens the front door, it comes out with a "HIGH" output to the buzzer after passing through the NOT gate. The buzzer will stop buzzing once the postman closes up the front door. The function of the buzzer is to notify the host instantly when there is postman inserting mails into the mailbox.

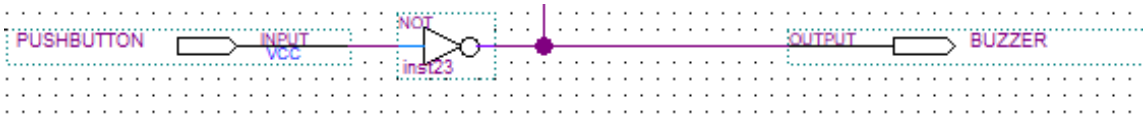

Figure 4. Block Diagram showing the circuit involving buzzer application

D. Pushbuttons

The DE2 board provides four pushbutton switches. Each of these switches is debounced using a Schmitt Trigger circuit. The four outputs called KEY[0], …, KEY[3] of the Schmitt Trigger device are connected directly to the Cyclone II FPGA. Each switch provides a high logic level (3.3 volts) when it is not pressed, and provides a low logic level (0 volts) when depressed. Since the pushbutton switches are debounced, they are appropriate for use as clock or reset inputs in a circuit.

In this project, we use the built-in pushbuttons to represent the front and back pushbuttons. We assign KEY[2] as the front pushbutton and KEY[0] as the back pushbutton which is also the reset button.

E. Using *Expansion* Header

The DE2 Board provides two 40-pin expansion headers. Each header connects directly to 36 pins on the Cyclone II FPGA, and also provides DC +5V (VCC5), DC +3.3V (VCC33), and two GND pins. Each pin on the expansion headers is connected to two diodes and a resistor that provide protection from high and low voltages. GPIO stands for General Purpose Input Output, which are connections between the FPGA and the real world.

In this project, we use the GPIO to connect the IR sensor, one Yellow LED, one Red LED and a buzzer. A breadboard is used for the prototype, 5V input voltage and Ground are connected to the external circuit from VCC5 and GND respectively.

4.0 RESULTS

We assign all the pins that require to the inputs and outputs of the circuit using the "Pin Planner" with reference to the DE2 User Manual.

Node Name	Direction	Location	I/O Bank	VREF Group	I/O Standard
7seg0	Output	PIN_T2	1	B1_N0	3.3-V LV...default)
7seg1	Output	PIN_P6	1	B1_N0	3.3-V LV...default)
7seg2	Output	PIN_P7	1	B1_N0	3.3-V LV...default)
7seg3	Output	PIN_T9	1	B1_N0	3.3-V LV...default)
7seg4	Output	PIN_R5	1	B1_N0	3.3-V LV...default)
7seg5	Output	PIN_R4	1	B1_N0	3.3-V LV...default)
7seg6	Output	PIN_R3	1	B1_N0	3.3-V LV...default)
B	Output	PIN_AE12	8	B8_N0	3.3-V LV...default)
BUZZER	Output	PIN_J22	5	B5_N0	3.3-V LV...default)
HIGH	Input	PIN_V2	1	B1_N0	3.3-V LV...default)
IR1	Input	PIN_D25	5	B5_N0	3.3-V LV...default)
LED0	Output	PIN_F24	5	B5_N0	3.3-V LV...default)
LED1	Output	PIN_AF22	7	B7_N0	3.3-V LV...default)
LED2	Output	PIN_W19	7	B7_N0	3.3-V LV...default)
LED3	Output	PIN_V18	7	B7_N0	3.3-V LV...default)
LED4	Output	PIN_U18	7	B7_N0	3.3-V LV...default)
LED5	Output	PIN_U17	7	B7_N0	3.3-V LV...default)
LED6	Output	PIN_AA20	7	B7_N0	3.3-V LV...default)
LED7	Output	PIN_E26	5	B5_N0	3.3-V LV...default)
LSB	Output	PIN_AE13	8	B8_N0	3.3-V LV...default)
MSB	Output	PIN_AD12	8	B8_N0	3.3-V LV...default)
PUSHBUTTON	Input	PIN_P23	6	B6_N0	3.3-V LV...default)
RESETSWITCH	Input	PIN_G26	5	B5_N0	3.3-V LV...default)

Figure 5. Pin Planner

After finishing the block diagram in QUARTUS II, the circuit is compiled to check for errors. Then proceed to the uploading of programme to the FPGA board using "Prorgammer". Testing of programme ran smoothly as the all the function needed performing well.

5.0 CONCLUSION

In conclusion, the objectives of the project are achieved. The proposed system of electronic mailbox using FPGA to detect letter has been presented. The mailbox work functionally to notify user for their new mail by buzzing the buzzer in their house, display the number mailbox opened or closed by postman and light up the LED at the mailbox. The mailbox is a user friendly, low cost and reliable. The system of the mailbox is designed using FPGA as FPGAs are reprogrammable and a concept can be verified in a hardware very fast, while in field-reconfiguration can keep up with future modifications without modifying the board layout.

However, the limitation on this system where the up- counter only counts from one until seven and stop after that. The counter won't count the number of mailbox opened or closed by postman after the seventh times. This is because the system is designed using 3-bit up-counter that counting from one to seven. If the system is design using 4-bit or 5-bit and above, the up counter will count until fifteen, thirty-one and above respectively. As the possibility for the number of mailbox to be opened or closed by postman in a week is low (not acceding to fifteen and above) the system is design using only 3-bits up counter and the counter will reset as the user collect their mail.

6.0 ACKNOWLEDGEMENT

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